Detector Arrays, Fabrication and Testing

Astronomy 525

Lecture 20

Outline

- Other PV detectors
- Detector Amplifiers
- CCDs
- Arrays of detectors/discrete detectors
- Detector Fabrication
  - Float Zone Processing
  - Epitaxial Growth
- Detector Testing
  - Hall Effect
  - Resistivity
  - Spreading Resistance
  - C-V measurements

Other Photovoltaic Detectors

- p-i-n photodiode
  - place an intrinsic region between p- and n-type regions
  - absorb light in intrinsic region
  - lower capacitance (faster operation)
- Avalanche photodiode
  - Operate at large negative bias voltage
  - photoexcited carriers accelerated to high energies
  - Inelastic scattering cause avalanche of elec.-hole pairs
  - G ~ 1000 possible

Not shown in class

The PIN Diode – 1

- The capacitance of the photodiode is reduced by widening the depletion region
- Furthermore, if the depletion region is so wide that most of the photoabsorption occurs there, then the photoexcited charge carriers are immediately swept along by the junction field, and the diffusion process no longer is important!
- Both process lead to improved frequency response
- The width of the depleting region can be increased by reducing the doping, but that leads to an undesirable decrease in R
- A better idea is to insert a high resistivity intrinsic layer between the p and n-doped regions: a PIN diode

Not shown in class

The PIN Diode – 2

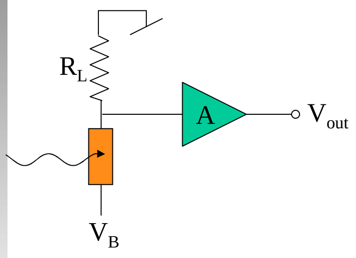
- Light is absorbed in the intrinsic region
  - The capacitance is greatly reduced by the intrinsic region
  - The response time is then given by:

$$\tau_{PIN} = l/\langle v_x \rangle = l/\{\mu_e \varepsilon_x\} = l^2/\{\mu_e(V_o+V_b)\}$$

- For silicon, $\mu_e \sim 1.35 \times 10^3$, and the high breakdown voltages enable operation with bias of 100 V. Therefore, a 1 mm thick intrinsic region would yield time constants of the order $\tau_{PIN} \sim 10^{-7}$ *seconds*.

Detector Amplifiers

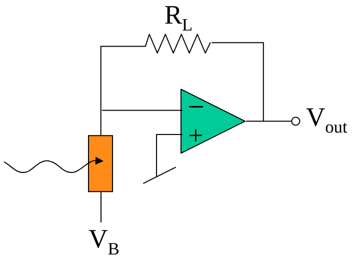
Source Follower



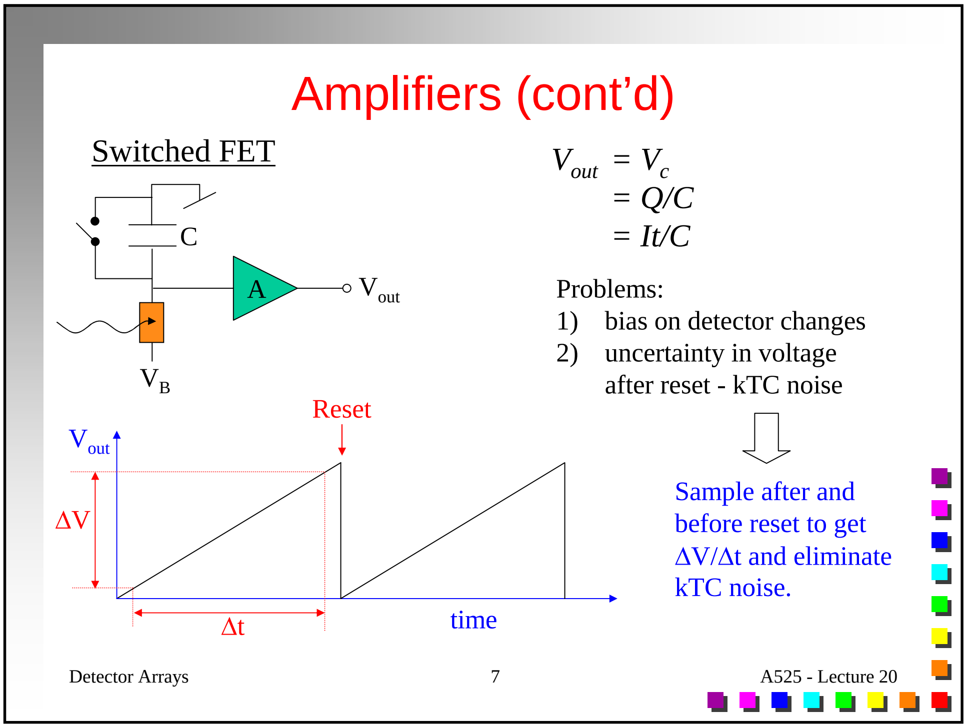
$V_{out} = I_D R_L$

but the bias voltage changes

TIA (Transimpedance Amplifier)



$V_{out} = - I_D R_L$



Amplifiers (cont'd)

Switched FET

$$V_{out} = V_c = Q/C = It/C$$

Problems:

1) bias on detector changes
2) uncertainty in voltage after reset - kTC noise

Sample after and before reset to get ΔV/Δt and eliminate kTC noise.

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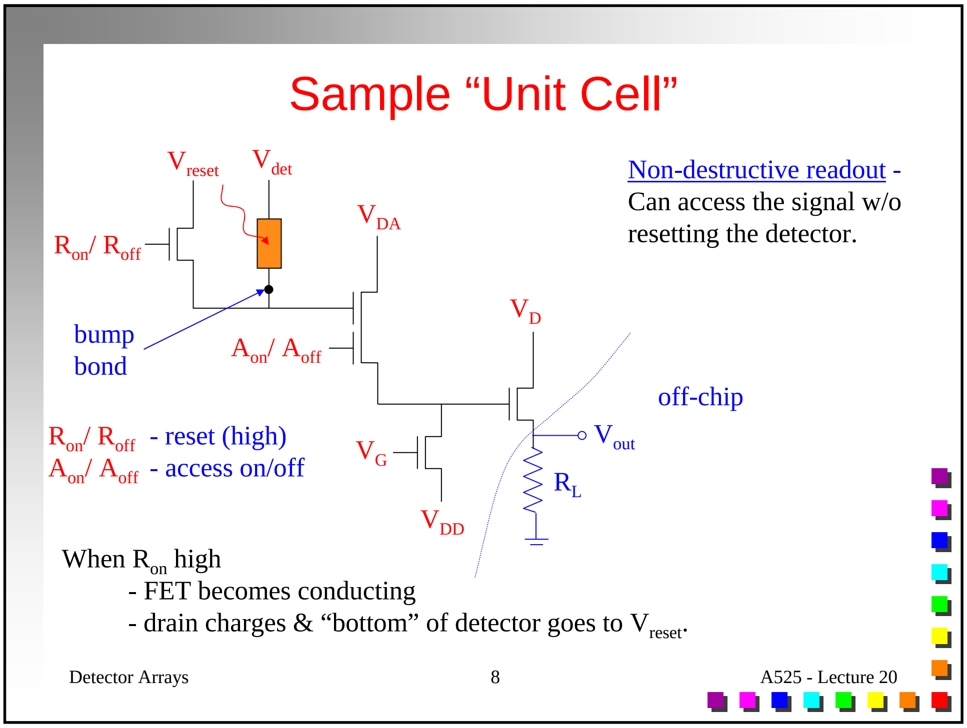

Sample "Unit Cell"

Non-destructive readout - Can access the signal w/o resetting the detector.

R_{on}/ R_{off} - reset (high)
A_{on}/ A_{off} - access on/off

When R_{on} high
- FET becomes conducting
- drain charges & "bottom" of detector goes to V_{reset}.

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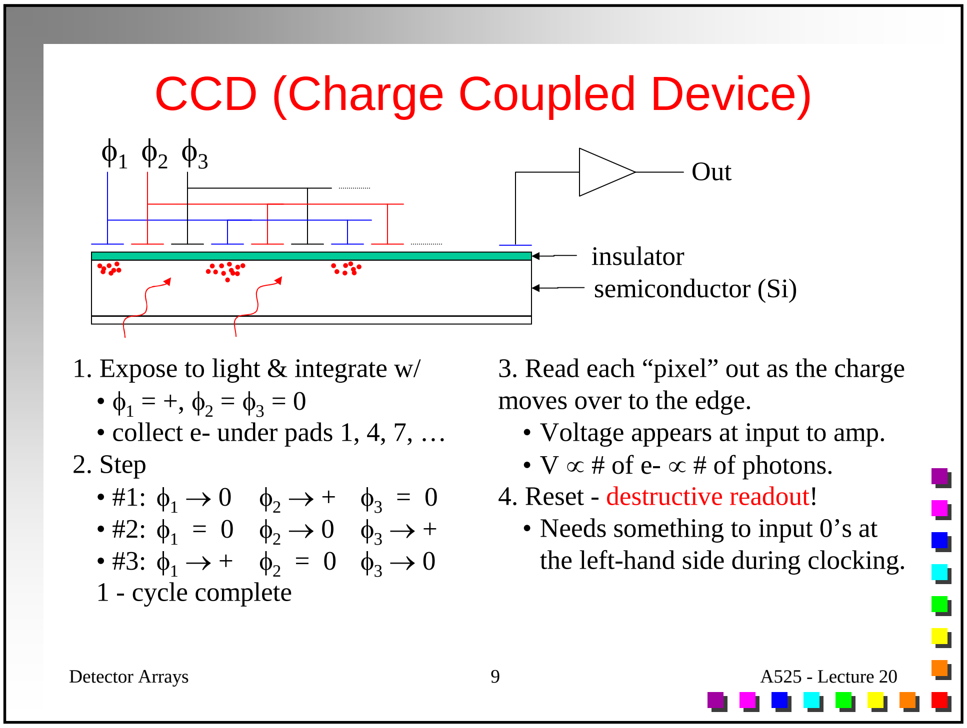
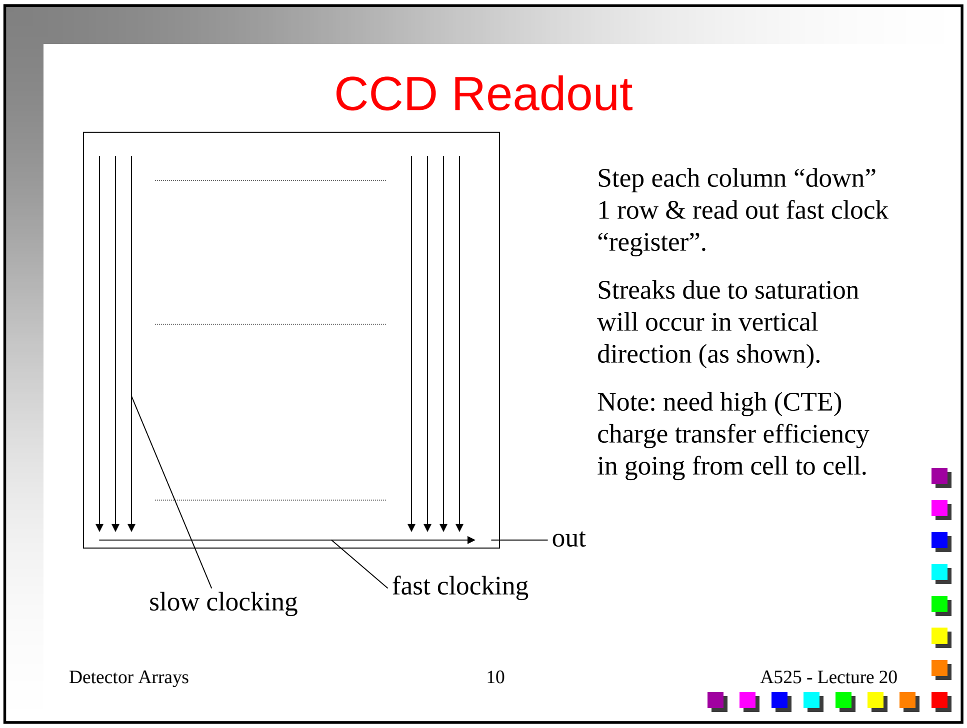


CCD (Charge Coupled Device)

1. Expose to light & integrate w/
   - $\phi_1 = +$, $\phi_2 = \phi_3 = 0$
   - collect e- under pads 1, 4, 7, …
2. Step
   - #1: $\phi_1 \rightarrow 0$ $\phi_2 \rightarrow +$ $\phi_3 = 0$
   - #2: $\phi_1 = 0$ $\phi_2 \rightarrow 0$ $\phi_3 \rightarrow +$
   - #3: $\phi_1 \rightarrow +$ $\phi_2 = 0$ $\phi_3 \rightarrow 0$

   1 - cycle complete
3. Read each "pixel" out as the charge moves over to the edge.
   - Voltage appears at input to amp.
   - $V \propto$ # of e- $\propto$ # of photons.
4. Reset - destructive readout!
   - Needs something to input 0's at the left-hand side during clocking.



CCD Readout

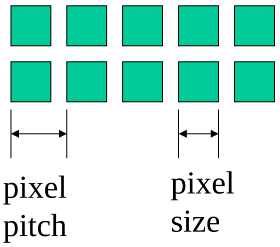
Step each column "down" 1 row & read out fast clock "register".

Streaks due to saturation will occur in vertical direction (as shown).

Note: need high (CTE) charge transfer efficiency in going from cell to cell.

Arrays of detectors

- Through photolithographic techniques, detectors and “contact” can be put down on a substrated w/ proper isolation to define individual elements.



$$\text{Fill factor} \equiv \frac{\text{Effective Area}}{\text{Total Area}}$$

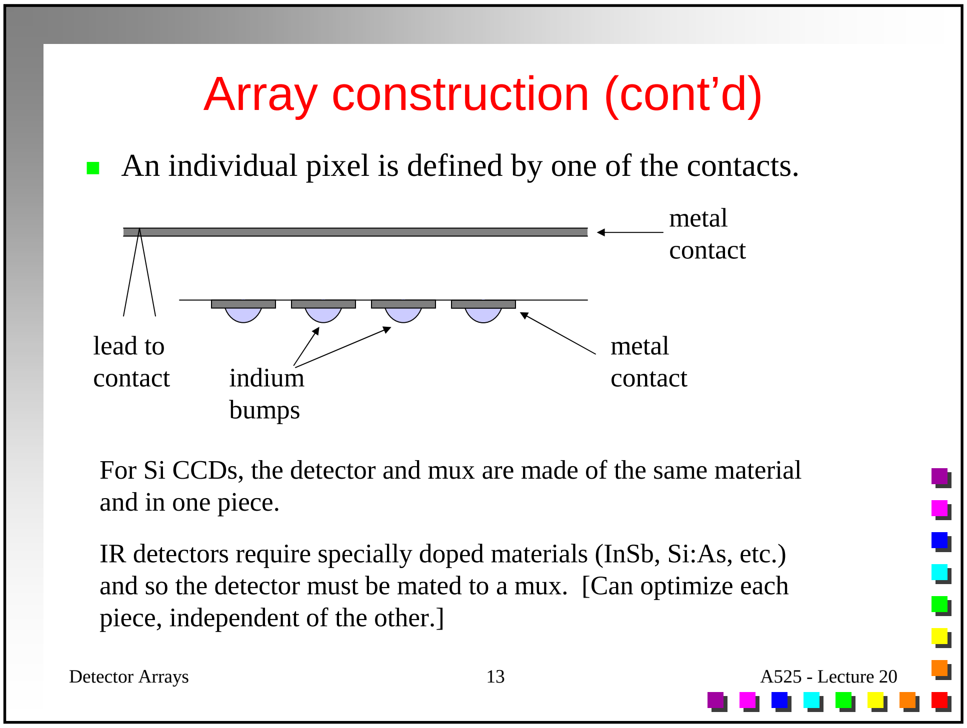
(> 85% is very good)

“Typical” array sizes:

- CCDs: 2048^2, 4096^2
- Near IR: 1024^2
- Mid IR: 256^2, 512^2, 1024^2

Array Construction

- We can envision two distinct components
  - detectors - optically active material
  - multiplexer - amplifier plus associated readout electronics
- Monolithic
  - detector and mux are made from the same piece of semiconductor, e.g. optical Si CCDs.
- Hybrid:
  - detector and mux are made separately
  - e.g. Si mux w/ Si, InSb, or HgCdTe detector
  - but each pixel much be connected to an output!

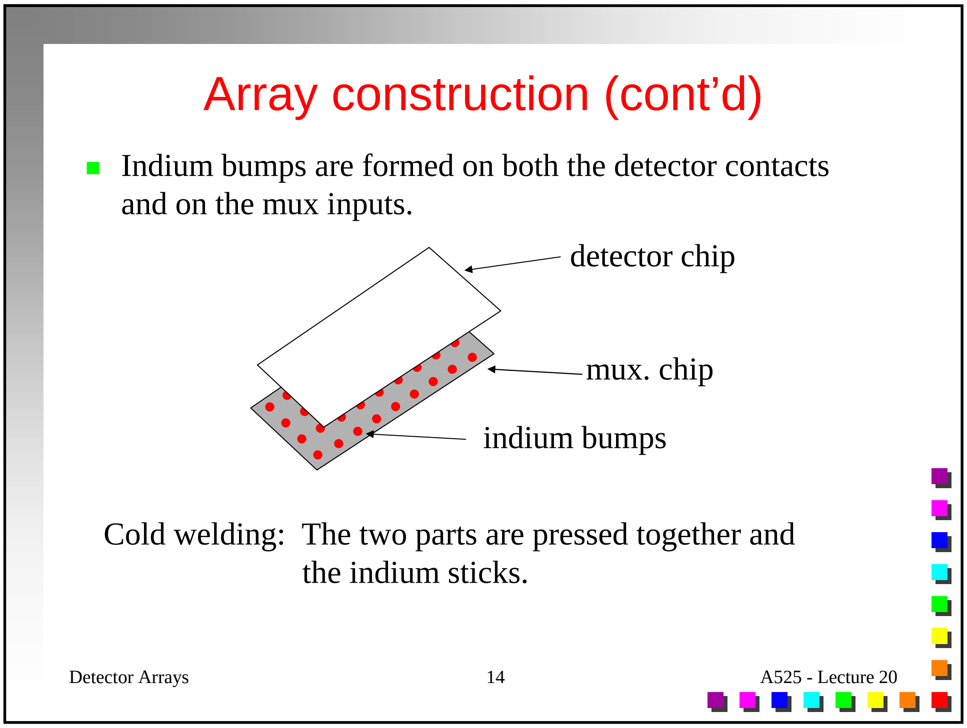


Array construction (cont’d)

- An individual pixel is defined by one of the contacts.

For Si CCDs, the detector and mux are made of the same material and in one piece.

IR detectors require specially doped materials (InSb, Si:As, etc.) and so the detector must be mated to a mux. [Can optimize each piece, independent of the other.]



Array construction (cont’d)

- Indium bumps are formed on both the detector contacts and on the mux inputs.

Cold welding: The two parts are pressed together and the indium sticks.

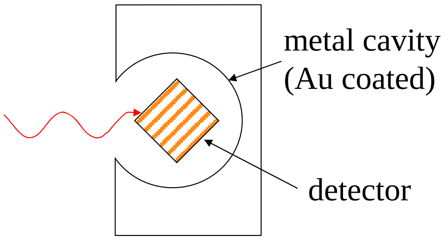
Current Array status

Type	Range (μm)	Size ($x \times y$)	R_N (e-)	i_d (e-/s)	Who
CCDs	0.35-1.0	> 4096	< 5	0	Ford
HgCdTe	0.9-2.5	2048	< 10	< 1	Teledyne
InSb	1.0-5.0	2048	< 10	< 1	Raytheon
Si:As BIB	5.0-27	128 – 256 256 – 1024	varies	< 10	DRS Tech, Raytheon
Si:Sb BIB	17-38	128 – 256	varies	< 50	DRS Tech
Ge:Ga	40-200	32 (discrete)	varies	---	Arizona, MPI

Discrete Devices

- Ge:Be $30 < \lambda < 50\ \mu$m
- Ge:Ga $50 < \lambda < 120\ \mu$m
- Stressed Ge:Ga $100 < \lambda < 200\ \mu$m

The integrating cavity -



For detector that are somewhat transparent - put in a cavity that reflects the non-absorbed radiation back to the detector.

Some References

- Physics of Semiconductor Devices, S. M. Sze, 1981.
  - Intrinsic, extrinsic, semiconductors
  - bipolar transistors, FET's, etc.
- Introduction to Solid State Physics, C. Kittel
  - "Readable" discussions of some of the physics of semiconductors
- The Infrared and Electro-Optical Systems Handbook
  - Vol 3: Electro-Optical Components (ed. W. D. Rogatto)
  - detectors, readouts, optics, cryogenics, etc.
- Radiometry and the Detector of Optical Radiation (Boyd)
  - Excellent book on theory
- Detection of light from UV to sub-mm (Rieke)
  - detectors, readout, etc.

Some definitions from Webster's

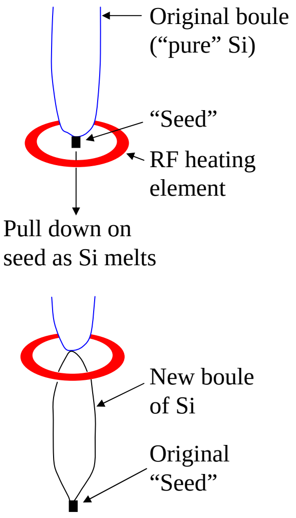
- boule (1918)
  - a pear-shaped mass formed synthetically in a special furnace with the atomic structure of a single crystal.
- epitaxy (1931)
  - the growth on a crystalline substrate of a crystalline substance that mimics the orientation of the substrate
- dopant (1962)
  - an impurity add usually in minute amounts to a pure substance to alter its properties

Detector Fabrication

- Float zone processing:
  - Fabricate a boule of doped Si and slice to make detectors
- Epitaxial Growth
  - Deposit doped Si on the surface of a crystal substrate

Material	atoms/cm^3
Si Crystal	5×10^{22}
PC As Doping	$\sim 2\text{-}5 \times 10^{16}$
BIB As Doping	$\sim 5 \times 10^{17}$
Impurity Acceptors	$< 2 \times 10^{12}$

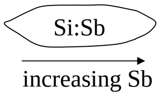
Float Zone Processing



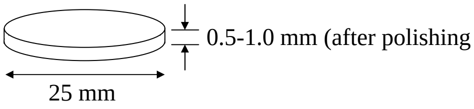
1. The Si boule is placed above an RF heating element and a "seed" crystal is touched to the boule.
2. The RF ring heat and melts the Si and as it drips a new boule is created. [This process "bubbles" out impurities, except Boron.]
3. Several passes are made to cleanse the Si.
4. In the last pass the dopant (i.e. Sb) is attached to the bottom of the boule.

Float Zone Processing (cont'd)

5. Dopant diffuses throughout the boule, but with a concentration gradient. By taking out a thin slice from somewhere along he boule, we can select the doping level.



6. The boule is cut with a fine-toothed saw and polished.



7. Contacts are ion implanted and the boule wafer is diced (cut) into small squares to make detectors.

Epitaxial Growth

- Epi - "on", taxis - "arrangement"
- Crystal growth by chemical reaction on the surface of a crystal. The thin layers have the same lattice structures as the original crystal, i.e.

$$SiCl_4 + 2H_2 \rightarrow Si\ (solid) + 4\ HCl\ (gas)$$

- Typical growth rate is 1 μm/min @ 1200 C with a mole fraction of 0.01% for $SiCl_4$.
- Impurities (for extrinsic Si production) can be introduced at this stage to generate the desired doping.

Passivation

- Prevents surface trapping
- Apply a “film” of material to the semiconductor surface that has a larger band gap to prevent the surface from being a potential well for carriers.
  - Usually an insulating layer, e.g. SiO_2, GeN
- This can also prevent the diffusion of impurities into the semiconductor.

Compensation

- Reduce the lifetime of carriers in photoconductors by adding acceptors or donors as appropriate.
  - This is to prevent avalanching
- Compensation:
  - Impurity has a different sign than the main dopant
- Counter Doping:
  - Impurity has the same sign, i.e. Cu doping in Ge:Ga
  - Neutral scattering

Hall Effect Testing

- Measures carrier concentration
  - In the presence of a magnetic field, a current flowing through the specimen generates a transverse electric field. The Hall coefficient is:

$$R_H = \frac{E_y}{j_x B} = -\frac{1}{ne}$$

j_x = current density
E_y = Hall field

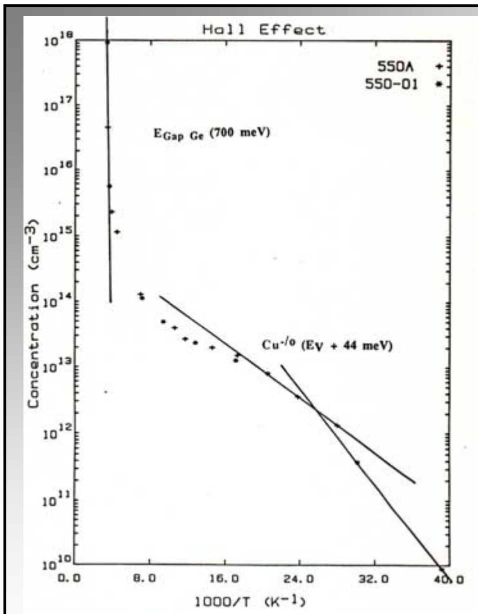
For free electron carriers

  - For two types of carriers:

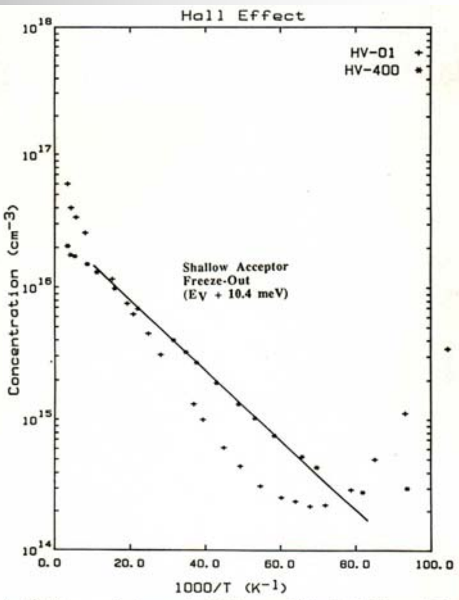
$$R_H = \frac{<\tau^2>}{<\tau>^2} \frac{p - b^2 n}{(p + bn)^2} \frac{1}{q}$$

b = μ_n/μ_p
τ = mean free time between carrier collisions

(See Kittel; Sze)



7. Variable temperature Hall effect measurements of a Ge epilayer on an n-type [113] substrate. The hole freeze-out curves indicate a light copper contamination. The two curves (+, *) are measurements of the same sample and demonstrate reproducibility.

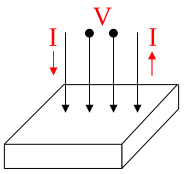


'ig. 18. Free carrier freeze-out of high energy B$^+$-implanted layer. Before annealing (+), the slope of the freeze-out curve is steeper than after annealing (•). The latter slope corresponds to ~10.4 meV, the binding energy of shallow boron acceptors. Below 15 K, hopping conduction becomes dominant.

Haller et. al (1989)

Resistivity Measurement Testing

- Use a 4 point probe.
  - Put a constant current in the outer probes and measure V on the inner two.

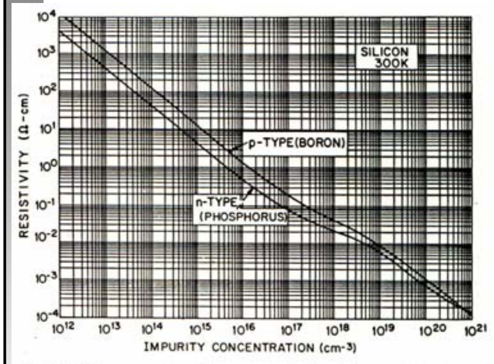


$$j = \sigma E$$

$$\rho = \frac{1}{\sigma} = \frac{1}{q(\mu_n n + \mu_p p)}$$

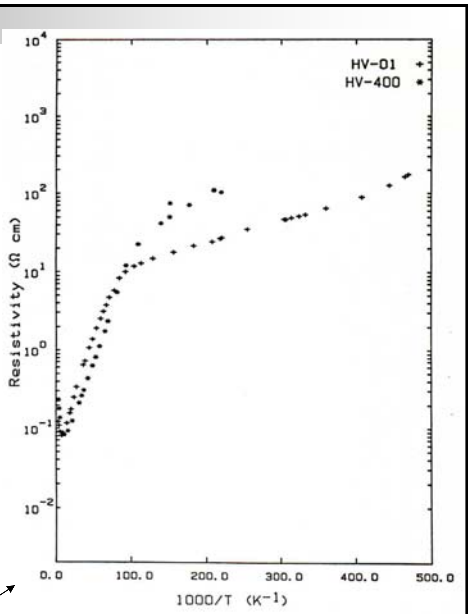
σ = conductivity
ρ = resistivity

Example Resistivities



21 Resistivity versus impurity concentration for silicon at 300 K. (After I

after Sze

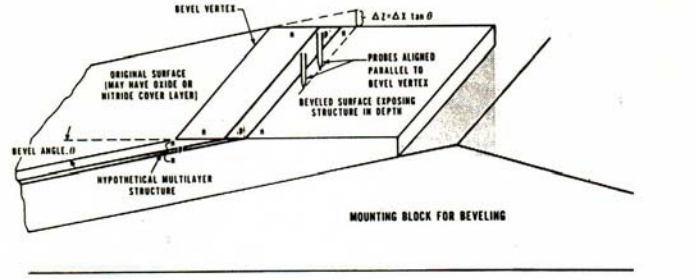


Haller et. al (1989)

Fig. 19. Resistivity as a function of inverse temperature of the high energy B+-implant layer before (+) and after (•) annealing. Hopping conduction becomes dominant below 15 K.

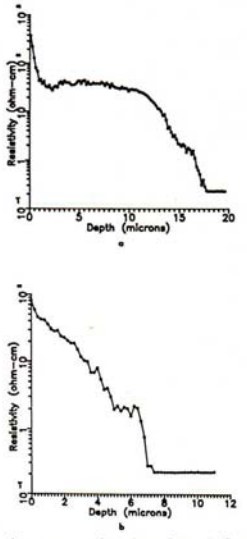
Spreading Resistance Analysis

- Measure resistivity as a function of depth into the sample.



15. Schematic of two probe depth profile measurements on an n/p/n structure beveled at angle Θ.

See “Two Proble (Spreading Resistance) Measurements for Evaluation of Semiconductor Devices” J.R. Ehrstein in *Nondestructive Evaluation of Semiconductor Devices and Materials*, ed. J.N. Zemel (1979).



Example SRA Measurement

Spreading resistance as a function of depth from the epilayer surface for: (a) an area of epilayer close to the leading edge of the wafer in II-16 where the growth rate was ~ 0.06 $\mu m\,min^{-1}$, and (b) an area of epilayer farthest from the leading edge of the same wafer where the growth rate was ~ 0.02 $\mu m\,min^{-1}$. The slight rise in resistivity at the very surface is due to the native oxide.

Haller et. al (1989)

C-V Measurements

- Capacitance (and size) of the depletion region in a BIB depends upon the bias
  - Thus the size of the depletion region can be measured
- Note:
  - The size of the depletion region at a given bias depends upon the acceptor (impurity) concentration.

Some References

- Boyd, R. 1983, *Radiometry and the Detection of Optical Radiation*
- Gillett, F.C., Dereniak, E.L., and Joyce, R.R. 1977, “Detectors for Infrared Astronomy,” Opt. Eng., **16**, 544-550.
- Gillett, F.C. 1987, “Infrared Arrays for Ground-based Astronomy,” in *Workshop on Ground-based Astronomical Observations with Infrared Detectors*, ed. G. Wynn-Williams.
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- Hudson, R.D., Jr. and Hudson, J.W. 1975, *Infrared Detectors*
  - Collection of papers on IR detectors
- Robinson, F.N.H. 1962, *Noise in Electrical Circuits*
- Barbe, D.F. 1975 “Imaging Devices using the Charge-Coupled Concept,” Proc. of IEEE, **63**, p. 38-67. [kTC noise]